19-3585; Rev 0; 2/05

# Nonvolatile, Dual, 8-Bit DACs with 2-Wire Serial Interface



## General Description

The MAX5109 dual 8-bit digital-to-analog converters (DACs) feature nonvolatile registers. These nonvolatile registers store the DAC operating modes and output states, allowing the DACs to initialize to specified configurations at power-up.

Precision on-chip output buffers swing rail-to-rail, and provide 8µs settling time. The I²C*-compatible, 2-wire serial interface allows for a maximum clock frequency of 400kHz.

The MAX5109 has independent high and low reference inputs allowing maximum output voltage range flexibility. The reference rails accept voltage inputs that range from ground to the positive supply rail.

This device operates from a single +2.7V to +5.25V supply and consumes 200µA per DAC. A software-controlled power-down mode decreases supply current to less than 25µA. A software-controlled mute mode sets each DAC, or both DACs simultaneously, to their respective REFL_ voltages. The MAX5109 also includes an asynchronous $\overline{\text{MUTE}}$ input, that drives both DAC outputs simultaneously to their respective REFL_ voltages.

The MAX5109 is available in a 16-pin QSOP and is specified for operation over the extended (-40°C to +85°C) temperature range.

## Applications

Digital Gain and Offset Adjustments

Programmable Attenuators

Portable Instruments

Power-Amp Bias Control

ATE Calibration

Laser Biasing

***Pin Configuration and Typical Operating Circuit appear at end of data sheet.***

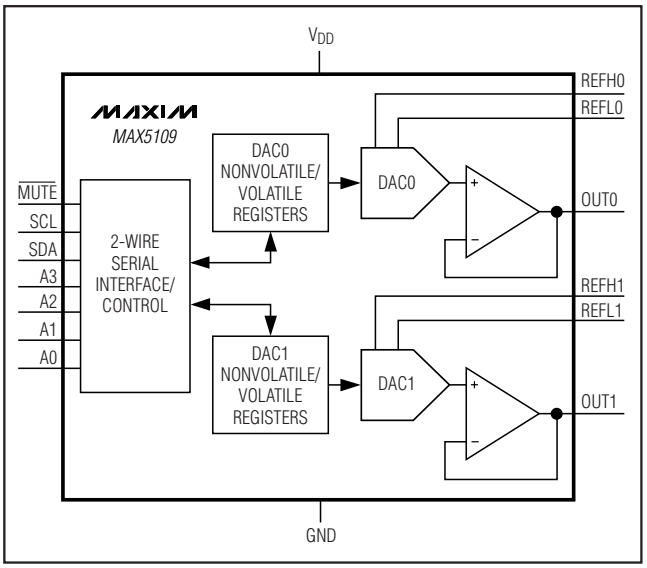
## Features

- **Nonvolatile Registers Initialize DACs to Stored States**
- **+2.7V to +5.25V Single-Supply Operation**
- **Dual 8-Bit DACs with Independent High and Low Reference Inputs**
- **Rail-to-Rail Output Buffers**
- **Low 200µA per DAC Supply Current**
- **Power-Down Mode Reduces Supply Current to 25µA (max)**
- **400kHz, I²C-Compatible, 2-Wire Serial Interface**
- **Asynchronous $\overline{\text{MUTE}}$ Input**
- **Small 16-Pin QSOP Package**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX5109EEE | -40°C to +85°C | 16 QSOP |

## Simplified Diagram

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# Nonvolatile, Dual, 8-Bit DACs with 2-Wire Serial Interface

## ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
$V_{DD}$, A0, A1, A2, A3, SCL, SDA, $\overline{MUTE}$.....-0.3V to +6.0V
OUT0, OUT1, REFH0, REFH1
REFL0, REFL1 .....-0.3V to ($V_{DD}$ + 0.3V)
Maximum Current into Any Pin .....±50mA
Power Dissipation ($T_A$ = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = +2.7V to +5.25V, GND = 0, REFH_ = $V_{DD}$, REFL_ = GND, $R_{LOAD}$ = 5kΩ, $C_L$ = 100pF, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{DD}$ = +3.0V and $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **STATIC ACCURACY** | | | | | | |
| Resolution | | | 8 | | | Bits |
| Integral Nonlinearity | INL | Code range 0A hex to F0 hex | | | ±1 | LSB |
| | | Full code range | | ±2 | | |
| Differential Nonlinearity (Note 2) | DNL | Code range 0A hex to F0 hex | | | ±0.5 | LSB |
| | | Full code range | | ±1 | | |
| Offset Error | ZCE | Code = 0A hex | | | ±20 | mV |
| Offset Temperature Coefficient | | Code = 0A hex | | ±20 | | µV/°C |
| Gain Error | | Code = F0 hex (Note 3) | | | ±1 | LSB |
| Gain-Error Temperature Coefficient | | Code = F0 hex | | ±0.002 | | LSB/°C |
| Power-Supply Rejection Ratio | PSRR | Code = FF hex or 0A hex, $V_{REFH\_}$ = 2.5V, $V_{REFL\_}$ = 0, f = DC | | | 1 | LSB/V |
| **REFERENCE INPUT (REFH_, REFL_)** | | | | | | |
| Input Voltage Range | $V_{REFH\_}$, $V_{REFL\_}$ | $V_{REFH\_} \geq V_{REFL\_}$ | 0 | | $V_{DD}$ | V |
| Input Resistance | | | 320 | 460 | 600 | kΩ |
| Input-Resistance Temperature Coefficient | | | | ±35 | | ppm/°C |
| Input Capacitance | | | | 10 | | pF |
| **DAC OUTPUTS (OUT_)** | | | | | | |
| Load Regulation | | Code = F0 hex, $R_{LOAD} \geq$ 5kΩ | | ±0.5 | ±1 | LSB |
| Output Leakage | | DAC powered down, not muted | | | ±10 | µA |
| Amplifier Output Resistance | | 0.5V ≤ $V_{OUT\_}$ ≤ ($V_{DD}$ - 0.5V) | | 0.5 | | Ω |
| **DIGITAL INPUTS (A_, $\overline{MUTE}$)** | | | | | | |
| Input High Voltage (Note 4) | $V_{IH}$ | 2.7V ≤ $V_{DD}$ < 3.6V | 0.7 x $V_{DD}$ | | | V |
| | | 3.6V ≤ $V_{DD}$ ≤ 5.25V | 2.52 | | | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +2.7V to +5.25V, GND = 0, REFH_ = $V_{DD}$, REFL_ = GND, $R_{LOAD}$ = 5kΩ, $C_L$ = 100pF, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{DD}$ = +3.0V and $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Input Low Voltage (Note 4) | $V_{IL}$ | 2.7V ≤ $V_{DD}$ < 3.6V | | | | 0.3 x $V_{DD}$ | V |
| | | 3.6V ≤ $V_{DD}$ ≤ 5.25V | | | | 1.1 | |
| Input Hysteresis | $V_{HYS}$ | | | | 0.05 x $V_{DD}$ | | V |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$ = 0 or $V_{DD}$ | | | | ±1 | µA |
| Input Capacitance | $C_{IN}$ | | | | 10 | | pF |
| **DIGITAL OUTPUT (SDA)** | | | | | | | |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 3mA | | | | 0.4 | V |
| | | $I_{SINK}$ = 6mA | | | | 0.6 | |
| Tri-State Leakage | $I_L$ | | | | | ±1 | µA |
| Tri-State Output Capacitance | $C_{OUT}$ | | | | 15 | | pF |
| **DYNAMIC PERFORMANCE** | | | | | | | |
| SCL to OUT_ Settling | $t_{COS}$ | (Note 5) | | | 8 | | µs |
| Crosstalk | | $V_{REFH\_}$ = 2.5$V_{P-P}$ at 10kHz (Note 6) | | | 55 | | dB |
| Multiplying Signal-to-Noise Plus Distortion | SINAD | $V_{REFH\_}$ = 2.5$V_{P-P}$ at 1kHz | | | 65 | | dB |
| | | $V_{REFH\_}$ = 2.5$V_{P-P}$ at 10kHz | | | 52 | | |
| Multiplying Bandwidth | | $V_{REFH\_}$ = 0.5$V_{P-P}$, 3dB bandwidth | | | 325 | | kHz |
| Reference Feedthrough | | $V_{REFH\_}$ = 2.5$V_{P-P}$ at f = 10kHz (Note 7) | | | 88 | | dB |
| Clock Feedthrough | | | | | 2.5 | | nVs |
| Output Noise | $e_N$ | | | | 800 | | nV/√Hz |
| Power-Up Time | $t_{SDR}$ | From power-down state | | | 4 | | µs |
| Power-Down Time | $t_{SDN}$ | | | | 1.5 | | µs |
| **INTERFACE PORTS (SCL, SDA)** | | | | | | | |
| Input Voltage | $V_{IL}$ | | | | | 0.3 x $V_{DD}$ | V |
| | $V_{IH}$ | | | 0.7 x $V_{DD}$ | | | |
| Input Hysteresis | $V_{HYS}$ | | | | 0.05 x $V_{DD}$ | | V |
| Input Current | $I_{IN}$ | | | | | ±1 | µA |
| Input Capacitance | $C_{IN}$ | | | | 5 | | pF |
| **POWER SUPPLIES** | | | | | | | |
| Power-Supply Voltage | $V_{DD}$ | | | 2.70 | | 5.25 | V |
| Supply Current | $I_{DD}$ | $I_{LOAD}$ = 0, digital inputs at GND or $V_{DD}$ | Normal operation | | 0.4 | 0.7 | mA |
| | | | During nonvolatile write | | | 2 | |
| Power-Down Current | | | | | | 25 | µA |

# Nonvolatile, Dual, 8-Bit DACs with 2-Wire Serial Interface

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +2.7V to +5.25V, GND = 0, REFH_ = $V_{DD}$, REFL_ = GND, $R_{LOAD}$ = 5kΩ, $C_L$ = 100pF, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{DD}$ = +3.0V and $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DIGITAL TIMING (Figure 3, Note 8)** | | | | | | |
| SCL Clock Frequency | $f_{SCL}$ | | | | 400 | kHz |
| Setup Time for START Condition | $t_{SU:STA}$ | | 0.6 | | | µs |
| Hold Time for START Condition | $t_{HD:STA}$ | | 0.6 | | | µs |
| SCL High Time | $t_{HIGH}$ | | 0.6 | | | µs |
| SCL Low Time | $t_{LOW}$ | | 1.3 | | | µs |
| Data Setup Time | $t_{SU:DAT}$ | | 100 | | | ns |
| Data Hold Time | $t_{HD:DAT}$ | | 0 | | 0.9 | µs |
| SDA, SCL Rise Time | $t_R$ | | | | 300 | ns |
| SDA, SCL Fall Time | $t_F$ | | | | 300 | ns |
| Setup Time for STOP Condition | $t_{SU:STO}$ | | 0.6 | | | µs |
| Bus Free Time Between a STOP and START Condition | $t_{BUF}$ | | 1.3 | | | µs |
| Pulse Width of Spike Suppressed | $t_{SP}$ | | | | 50 | ns |
| Maximum Capacitive Load for Each Bus Line | $C_B$ | (Note 9) | | 400 | | pF |
| Write NV Register Busy Time | | (Note 10) | | | 15 | ms |
| **NONVOLATILE MEMORY RELIABILITY** | | | | | | |
| Data Retention | | $T_A$= +85°C | | 50 | | Years |
| Endurance | | $T_A$= +25°C | | 200,000 | | Stores |
| | | $T_A$= +85°C | | 50,000 | | |

**Note 1:** All devices are 100% production tested at $T_A$ = +25°C. All temperature limits are guaranteed by design.

**Note 2:** Guaranteed monotonic.

**Note 3:** Gain error is defined as:

$$\frac{256 \times (V_{F0,Meas} - ZCE - V_{F0,Ideal})}{V_{REFH\_}}$$

where $V_{F0,Meas}$ is the DAC voltage with input code F0 hex and $V_{F0,Ideal}$ is the ideal DAC voltage with input code F0 hex or ($V_{REFH}$ - $V_{REFL}$) x (240 / 256) + $V_{REFL}$.

**Note 4:** The device draws higher supply current when the digital inputs are driven with voltages between ($V_{DD}$ - 0.5V) and (GND + 0.5V). See Supply Current vs. Digital Input Voltage in the *Typical Operating Characteristics*.

**Note 5:** Output settling time is measured from the 50% point of the rising edge of the last SCL of the data byte to 0.5 LSB of OUT_'s final value for a code transition from 10 hex to F0 hex.

**Note 6:** Crosstalk is defined as the coupling from a DAC switching from code 00 hex to code FF hex to any other DAC that is in a steady state at code 00 hex.

**Note 7:** Reference feedthrough is defined as the coupling from one driven reference with input code = FF hex to any other DAC output with the reference of the DAC at a constant value and input code = 00 hex.

**Note 8:** SCL clock period includes rise and fall times $t_R$ and $t_F$. All digital input signals are specified with $t_R$ = $t_F$ = 2ns and timed from a voltage level of ($V_{IL}$ + $V_{IH}$) / 2.

**Note 9:** An appropriate bus pullup resistance must be selected depending on board capacitance. Refer to the document linked to this web address: www.semiconductors.philips.com/acrobat/literature/9398/39340011.pdf.

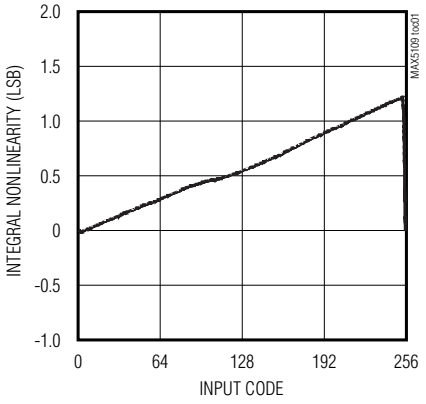
**Note 10:** The busy time begins from the initiation of the stop pulse.

# Nonvolatile, Dual, 8-Bit DACs with 2-Wire Serial Interface

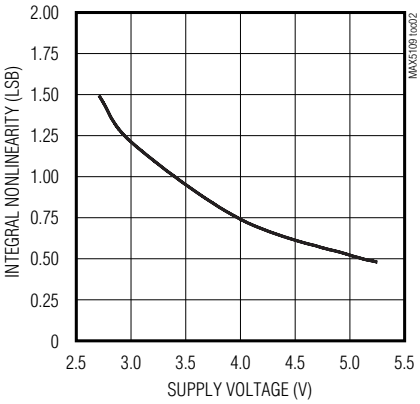
## Typical Operating Characteristics

($V_{DD}$ = +3V, $V_{REFH\_}$ = +3V, $V_{REFL\_}$ = GND, $R_L$ = 5kΩ, $C_L$ = 100pF, $T_A$ = +25°C, unless otherwise noted.)

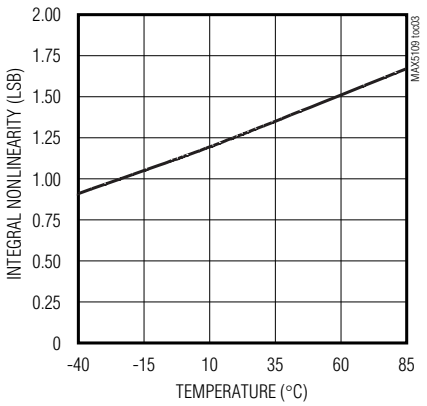
**INTEGRAL NONLINEARITY vs. INPUT CODE**



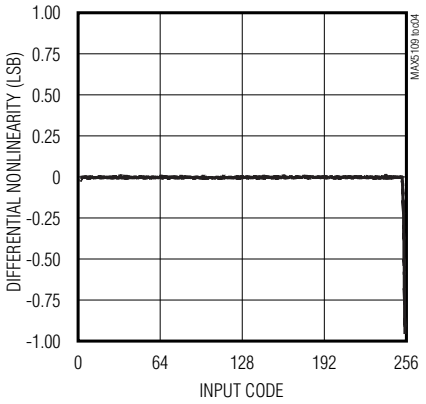

**INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE**



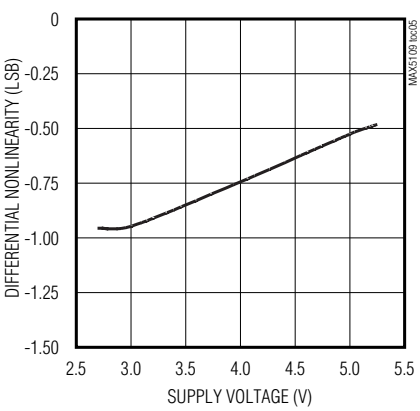

**INTEGRAL NONLINEARITY vs. TEMPERATURE**



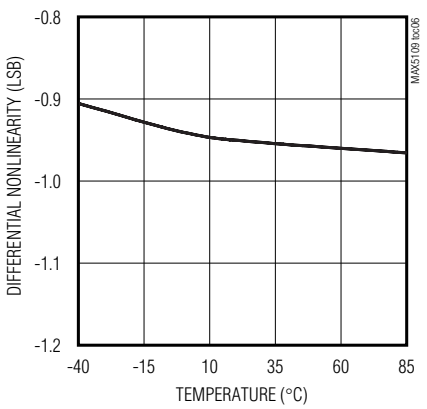

**DIFFERENTIAL NONLINEARITY vs. INPUT CODE**



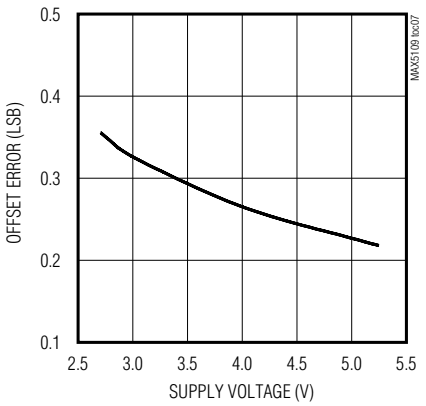

**DIFFERENTIAL NONLINEARITY vs. SUPPLY VOLTAGE**



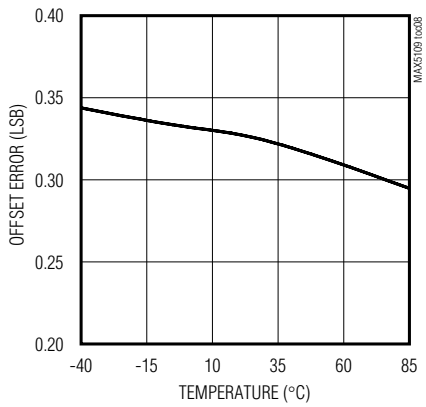

**DIFFERENTIAL NONLINEARITY vs. TEMPERATURE**



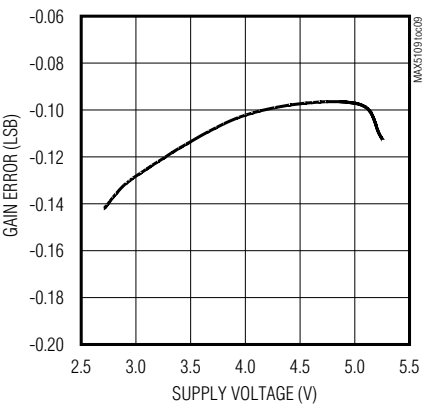

**OFFSET ERROR vs. SUPPLY VOLTAGE**




**OFFSET ERROR vs. TEMPERATURE**




**GAIN ERROR vs. SUPPLY VOLTAGE**

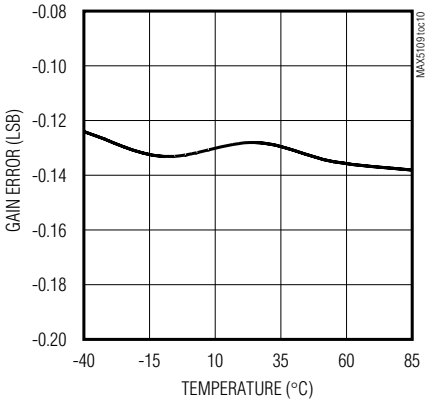


# Nonvolatile, Dual, 8-Bit DACs with 2-Wire Serial Interface

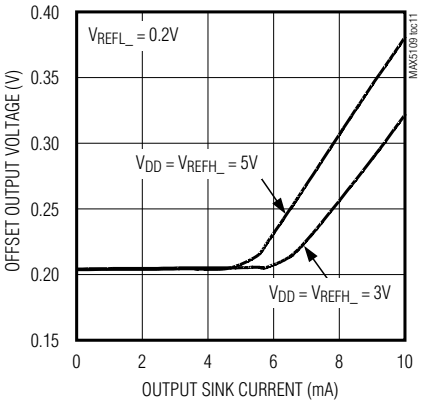
## Typical Operating Characteristics (continued)

($V_{DD}$ = +3V, $V_{REFH\_}$ = +3V, $V_{REFL\_}$ = GND, $R_L$ = 5kΩ, $C_L$ = 100pF, $T_A$ = +25°C, unless otherwise noted.)

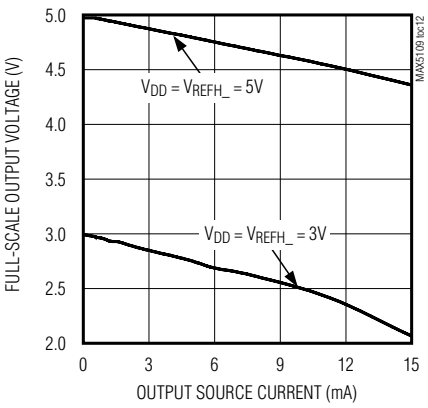
**GAIN ERROR vs. TEMPERATURE**



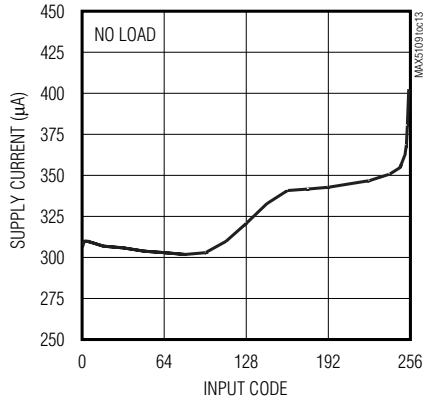

**OFFSET OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT**



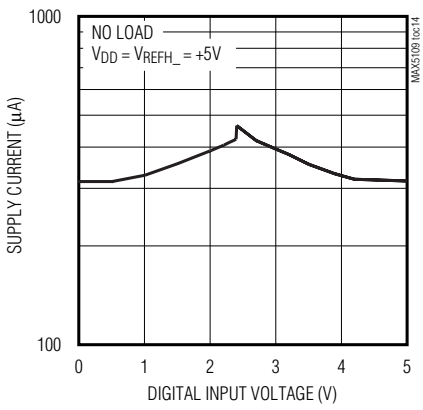

**FULL-SCALE OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT**



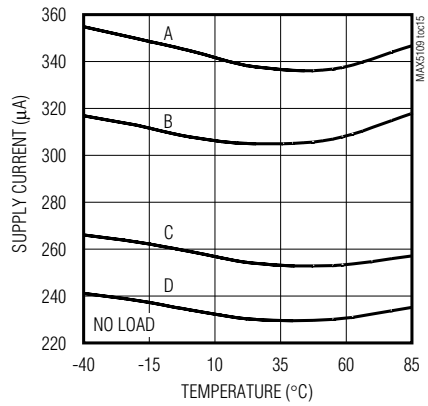

**SUPPLY CURRENT vs. INPUT CODE**




**SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE**




**SUPPLY CURRENT vs. TEMPERATURE**

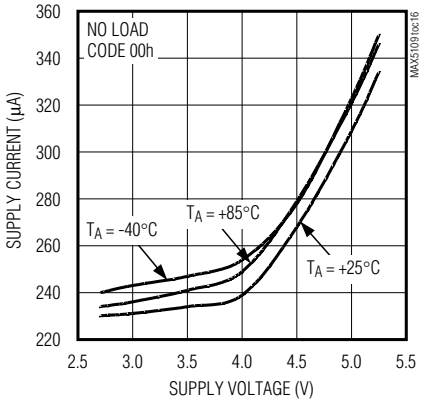



A: $V_{DD}$ = 5V, $V_{REFH\_}$ = 4.096V, CODE = FFh
B: $V_{DD}$ = 5V, $V_{REFH\_}$ = 4.096V, CODE = 00h
C: $V_{DD}$ = 3V, $V_{REFH\_}$ = 2.5V, CODE = FFh
D: $V_{DD}$ = 3V, $V_{REFH\_}$ = 2.5V, CODE = 00h

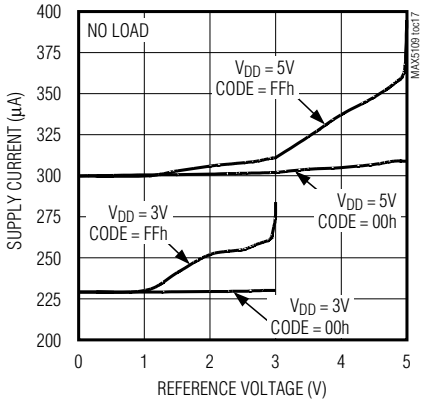
## Typical Operating Characteristics (continued)

($V_{DD}$ = +3V, $V_{REFH\_}$ = +3V, $V_{REFL\_}$ = GND, $R_L$ = 5kΩ, $C_L$ = 100pF, $T_A$ = +25°C, unless otherwise noted.)

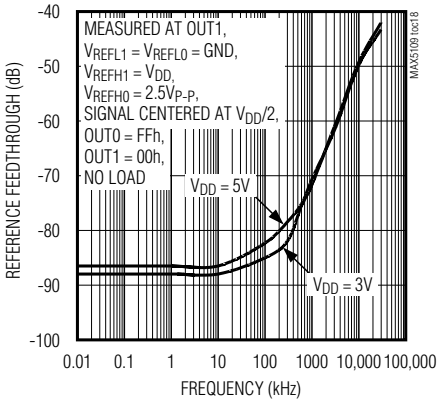
**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



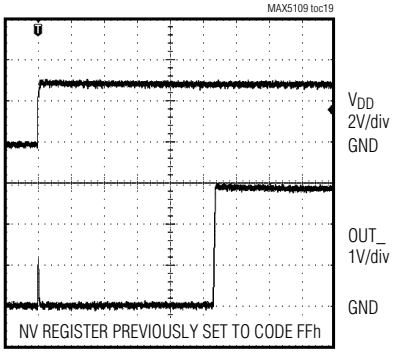

**SUPPLY CURRENT vs. REFERENCE VOLTAGE**



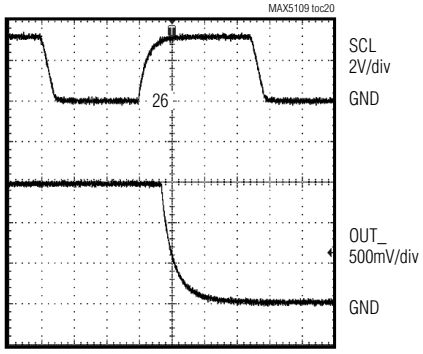

**REFERENCE FEEDTHROUGH vs. FREQUENCY**



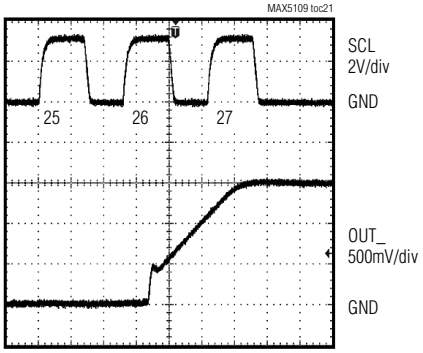

**STARTUP GLITCH**



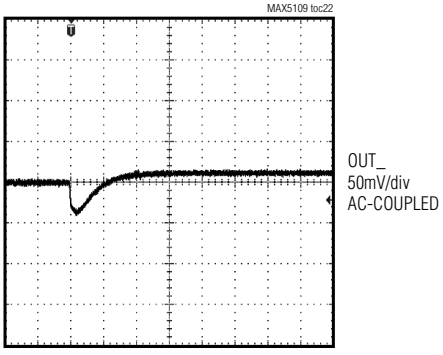

**POWER-DOWN TRANSITION**



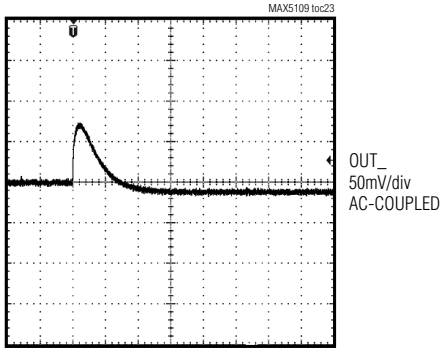

**POWER-UP TRANSITION**



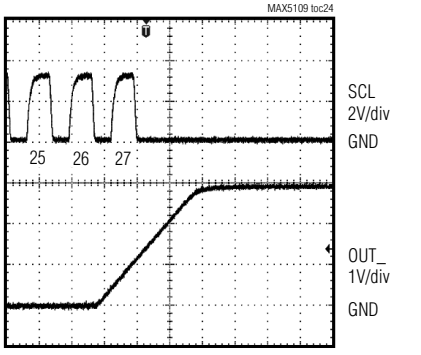

**POSITIVE CARRY TRANSITION**




**NEGATIVE CARRY TRANSITION**




**POSITIVE SETTLING TIME**

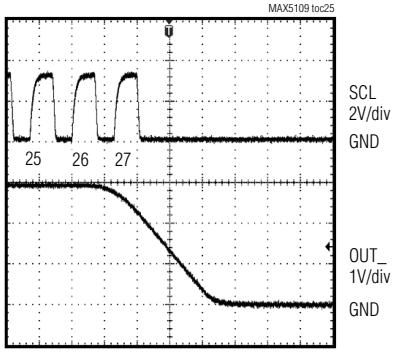


# Nonvolatile, Dual, 8-Bit DACs with 2-Wire Serial Interface

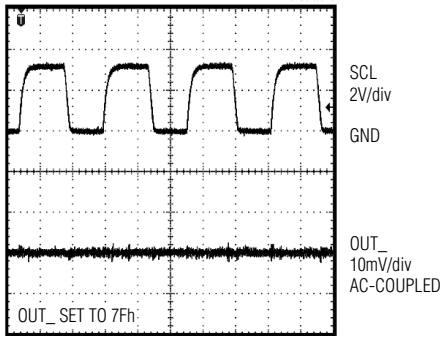
## Typical Operating Characteristics (continued)

($V_{DD}$ = +3V, $V_{REFH\_}$ = +3V, $V_{REFL\_}$ = GND, $R_L$ = 5kΩ, $C_L$ = 100pF, $T_A$ = +25°C, unless otherwise noted.)

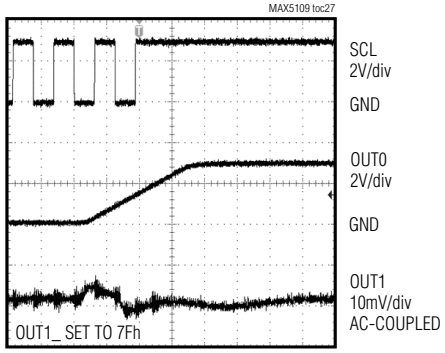
**NEGATIVE SETTLING TIME**




**CLOCK FEEDTHROUGH**




**OUTPUT CROSSTALK**




## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | A3 | Address Select 3. Connect to $V_{DD}$ or GND to set the device address. |
| 2 | A2 | Address Select 2. Connect to $V_{DD}$ or GND to set the device address. |
| 3 | A1 | Address Select 1. Connect to $V_{DD}$ or GND to set the device address. |
| 4 | A0 | Address Select 0. Connect to $V_{DD}$ or GND to set the device address. |
| 5 | REFH1 | DAC1 High Reference Input. REFH1 must be equal to or greater than REFL1. |
| 6 | REFL1 | DAC1 Low Reference Input. REFL1 must be equal to or less than REFH1. |
| 7 | OUT1 | DAC1 Output. OUT1 is buffered with a unity-gain amplifier. |
| 8 | GND | Ground |
| 9 | $\overline{MUTE}$ | Active-Low Mute Input. Connect $\overline{MUTE}$ low to drive all DAC outputs to their respective reference low voltages. Connect $\overline{MUTE}$ to $V_{DD}$ for normal operation. |
| 10 | N.C. | No Connection. Not internally connected. |
| 11 | OUT0 | DAC0 Output. OUT0 is buffered with a unity-gain amplifier. |
| 12 | REFL0 | DAC0 Low Reference Input. REFL0 must be equal to or less than REFH0. |
| 13 | REFH0 | DAC0 High Reference Input. REFH0 must be equal to or greater than REFL0. |
| 14 | SCL | Serial Clock Input. Connect SCL to $V_{DD}$ through a 2.4kΩ pullup resistor. |
| 15 | $V_{DD}$ | Positive Power Input. Connect $V_{DD}$ to a +2.7 to +5.25V power supply. Bypass $V_{DD}$ to GND with a 0.1µF capacitor as close to the device as possible. |
| 16 | SDA | Serial Data Input/Output. Connect SDA to $V_{DD}$ through a 2.4kΩ pullup resistor. |

# Nonvolatile, Dual, 8-Bit DACs with 2-Wire Serial Interface

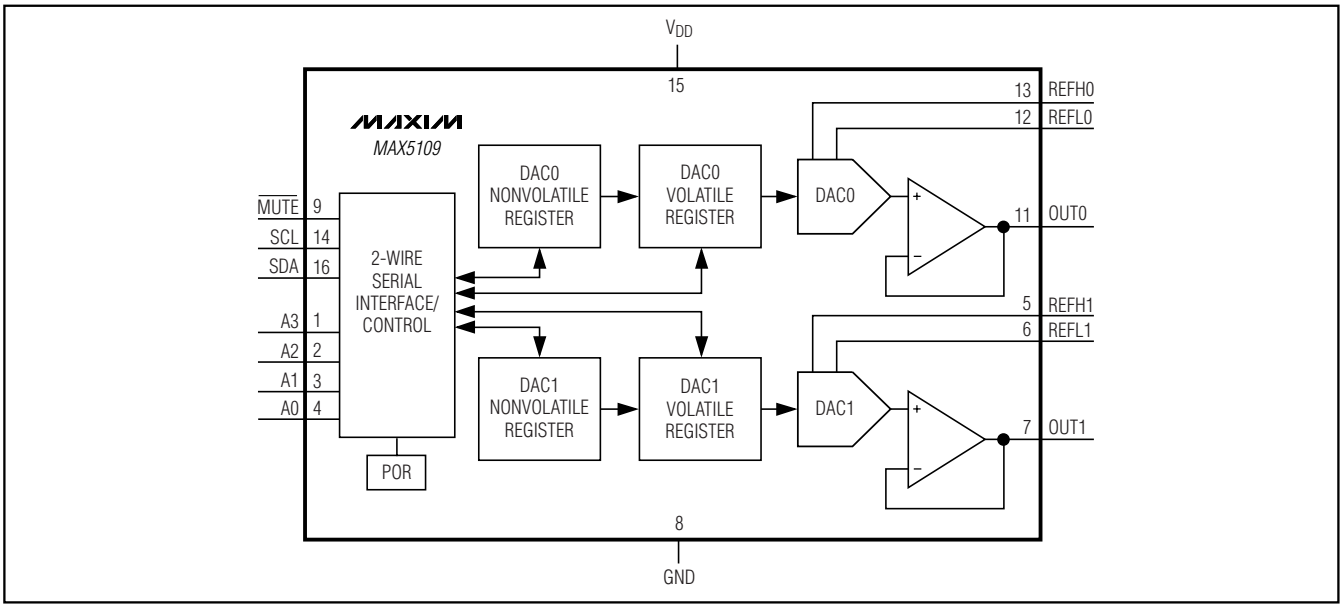



*Figure 1. MAX5109 Functional Diagram*

## Detailed Description

The MAX5109 8-bit DACs feature internal, nonvolatile registers that store the DAC states for initialization during power-up. This device consists of resistor-string DACs, rail-to-rail output buffers, a shift register, power-on reset (POR) circuitry, and volatile and nonvolatile memory registers (Figure 1). The shift register decodes the control and address bits, routing the data to the proper registers. Writing data to a selected volatile register immediately updates the DAC outputs.

The volatile registers retain data as long as the device is powered. Removing power clears the volatile registers. The nonvolatile registers retain data even after power is removed. On startup, when power is first applied, data from the nonvolatile registers is transferred to the volatile registers to automatically initialize the device. Read data from the nonvolatile or volatile registers using the 2-wire serial interface.

### DAC Operation

The MAX5109 uses a DAC matrix decoding architecture that saves power. A resistor string divides the difference between the external reference voltages, $V_{REFH\_}$ and $V_{REFL\_}$. Row and column decoders select the appropriate tap from the resistor string, providing the equivalent analog voltage. The resistor string presents a code-independent input impedance to the reference and guarantees a monotonic output. Figure 2 shows a simplified diagram of one DAC.

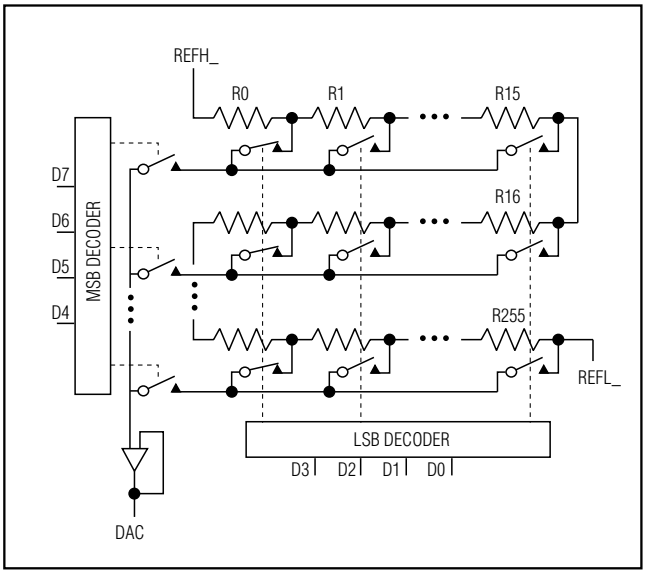



*Figure 2. DAC Simplified Circuit Diagram*

### Output Buffer Amplifiers

The MAX5109 analog outputs are internally buffered by precision unity-gain amplifiers. The outputs swing from GND to $V_{DD}$ with a $V_{REFL\_}$-to-$V_{REFH\_}$ output transition. The amplifier outputs typically settle to ±0.5 LSB in 8µs when loaded with 5kΩ in parallel with 100pF.

# Nonvolatile, Dual, 8-Bit DACs with 2-Wire Serial Interface

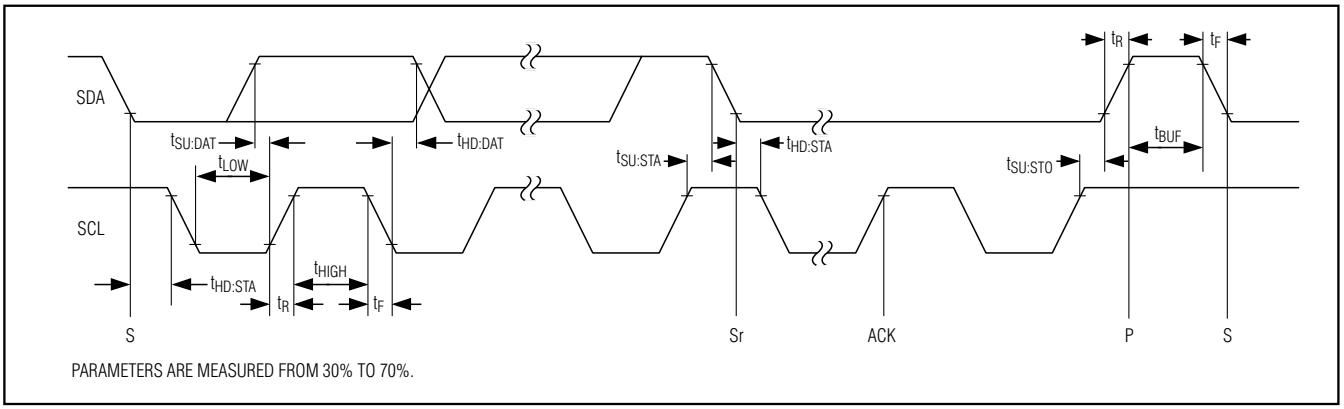



*Figure 3. 2-Wire Serial-Interface Timing Diagram*

### DAC Registers

The MAX5109 features two registers per DAC, a volatile and a nonvolatile register, that store the DAC data. The volatile DAC register holds the current value of each DAC. Write data to the volatile registers directly from the 2-wire serial interface or by loading the previously stored data from the respective nonvolatile register. Clear the volatile registers by removing power to the device. The volatile registers are read/write.

The nonvolatile register retains the DAC values even after power is removed. Read stored data using the 2-wire serial interface. On power-up, the device is automatically initialized with data stored in the nonvolatile registers. The nonvolatile registers are read/write and programmed to all zeros at the factory.

## Serial Interface

The MAX5109 features an I²C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX5109 and the master at rates up to 400kHz (Figure 3). The master (typically a microcontroller) initiates data transfer on the bus and generates SCL. SDA and SCL require pullup resistors (2.4kΩ or greater; see the *Typical Operating Circuit*). Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot of the bus signals.

### I²C Compatibility

The MAX5109 is compatible with existing I²C systems. SCL and SDA are high-impedance inputs; SDA has an open-drain output. The *Typical Operating Circuit* shows an I²C application. The communication protocol supports standard I²C 8-bit communications. The general call address is ignored, and CBUS formats are not supported. The device's address is compatible with 7-bit I²C addressing protocol only. No 10-bit address formats are supported.

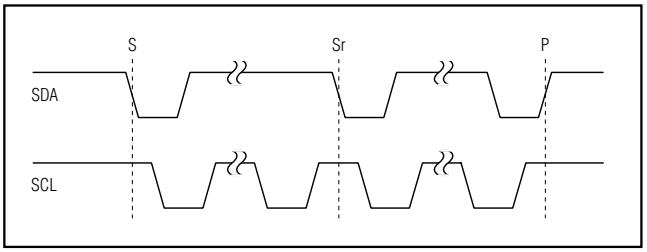



*Figure 4. START and STOP Conditions*

### Bit Transfer

One data bit transfers during each SCL rising edge. Nine clock cycles are required to transfer the data into or out of the MAX5109. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are read as control signals (see the *START and STOP Conditions* section). Both SDA and SCL idle high.

### START and STOP Conditions

The master initiates a transmission with a START condition (S), a high-to-low transition on SDA with SCL high. The master terminates a transmission with a STOP condition (P), a low-to-high transition on SDA while SCL is high (Figure 4). A START condition from the master signals the beginning of a transmission to the MAX5109. The master terminates transmission by issuing a STOP condition. The STOP condition frees the bus. If a REPEATED START condition (Sr) is generated instead of a STOP condition, the bus remains active.

### Early STOP Conditions

The MAX5109 recognizes a STOP condition at any point during transmission except if a STOP condition occurs in the same high pulse as a START condition (Figure 5). This condition is not a legal I²C format.

### REPEATED START Conditions

A REPEATED START (Sr) condition is used when the bus master is writing to several I²C devices and does not want to relinquish control of the bus. The MAX5109 serial interface supports continuous write operations with an Sr condition separating them. Continuous read operations require Sr conditions because of the change in direction of data flow.

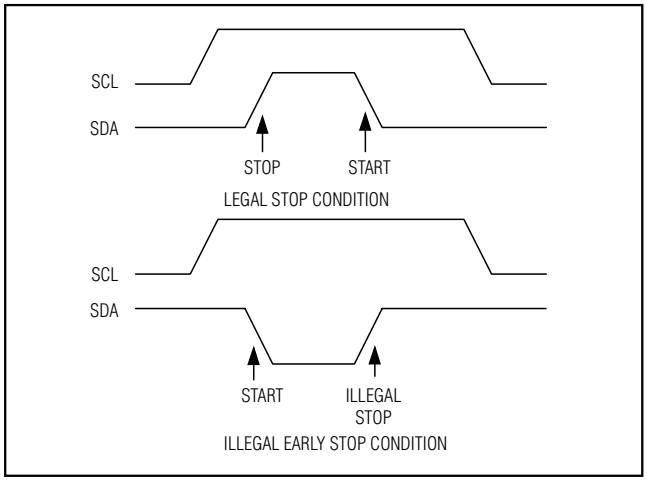



*Figure 5. Early STOP Conditions*

### Acknowledge Bit (ACK) and Not-Acknowledge Bit (NACK)

Successful data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX5109 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse (Figure 6). To generate a not acknowledge, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the master should reattempt communication at a later time.

### Slave Address

A master initiates communication with a slave device by issuing a START condition followed by a slave address (Figure 7). The slave address consists of 7 address bits and a read/write bit (R/$\overline{W}$). When idle, the device continuously waits for a START condition followed by its slave address. When the device recognizes its slave address, it acquires the data byte and executes the command. The first 3 bits (MSBs) of the slave address have been factory programmed and are always 010. Connect A3–A0 to $V_{DD}$ or GND to program

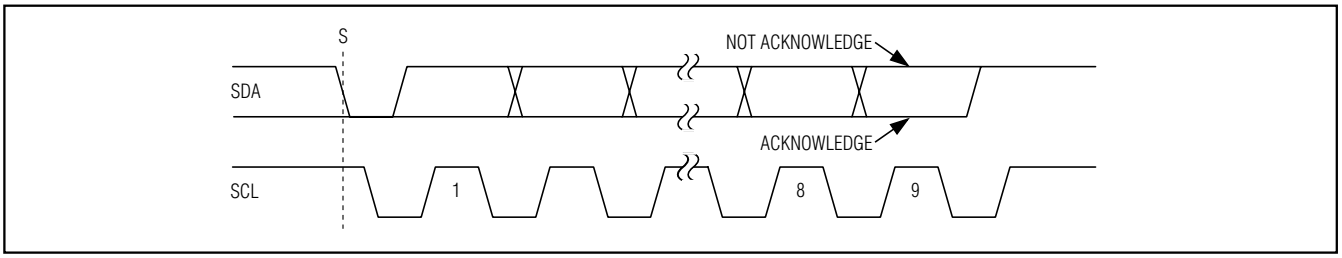



*Figure 6. Acknowledge and Not-Acknowledge Bits*

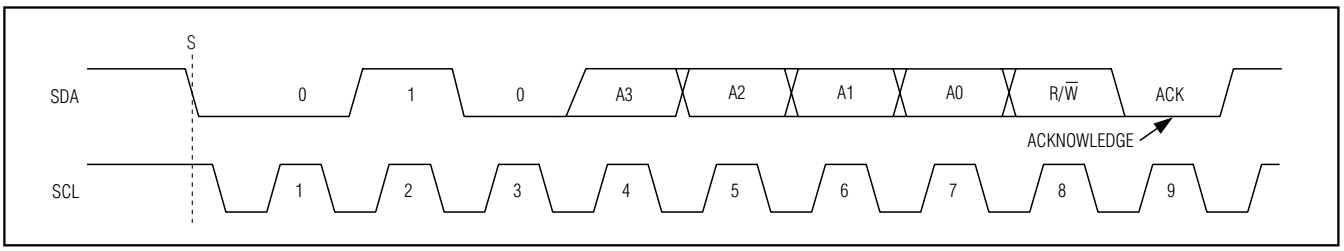



*Figure 7. Slave Address Byte*

# Nonvolatile, Dual, 8-Bit DACs with 2-Wire Serial Interface

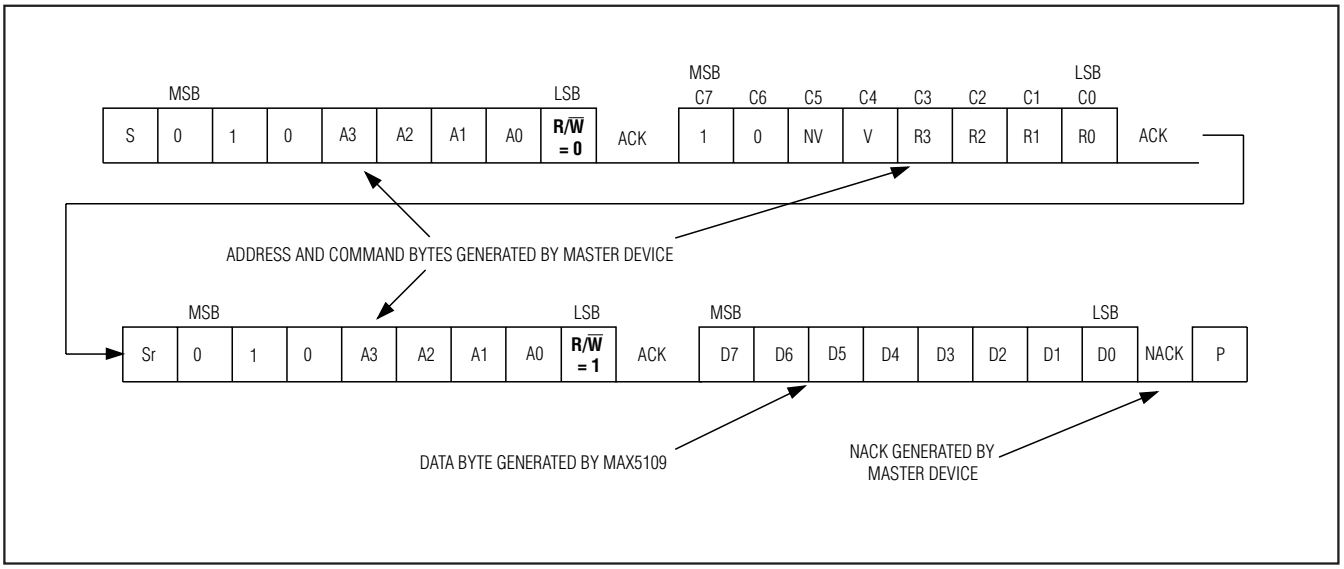



*Figure 8. Example Read Word Data Sequence*

the remaining 4 bits of the slave address. The least significant bit (LSB) of the address byte (R/$\overline{W}$) determines whether the master is writing to or reading from the MAX5109. (R/$\overline{W}$ = 0 selects a write condition. R/$\overline{W}$ = 1 selects a read condition.) After receiving the address, the MAX5109 (slave) issues an acknowledge by pulling SDA low for one clock cycle.

### Write Cycle

The write command requires 27 clock cycles. In write mode (R/$\overline{W}$ = 0), the command byte that follows the address byte controls the MAX5109 (Table 1). For a write function, set bits C7 and C6 to zero. Set bits C5 and C4 to select the volatile or nonvolatile register (Table 2). Set bits C3–C0 to select the respective DAC register (Table 3). The registers update on the rising edge of the 26th SCL pulse. Prematurely aborting the write cycle does not update the DAC. See Table 4 for a summary of the write commands.

### Read Cycle

A read command requires 36 clock cycles. In read mode, the MAX5109 sends the contents of the volatile and nonvolatile registers to the bus. Reading a register requires a REPEATED START (Sr) condition. To read a register first, write a read command (R/$\overline{W}$ = 0, Figure 8). Set the most significant 2 bits of the command byte to 10 (C7 = 1 and C6 = 0). Set bits C5 and C4 to read from either the volatile or nonvolatile register (Table 5). Set bits C3–C0 to select the desired DAC register (Table 6). After the command byte, send a Sr condition followed by the address of the device (R/$\overline{W}$ = 1). The MAX5109 then acknowledges and sends the data to the bus.

## Table 1. Write Operation

| | START | ADDRESS BYTE | | | | | | | | | COMMAND BYTE | | | | | | | | | DATA BYTE | | | | | | | | | STOP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | R/$\overline{W}$ | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| Master SDA | S | 0 | 1 | 0 | A3 | A2 | A1 | A0 | 0 | | C7 | C6 | NV | V | R3 | R2 | R1 | R0 | | D7–D0 | | | | | | | | | P |
| Slave SDA | | | | | | | | | | ACK | | | | | | | | | ACK | | | | | | | | | ACK | |

### Table 2. Volatile and Nonvolatile Write Selection

| NONVOLATILE (NV) | VOLATILE (V) | FUNCTION |
|---|---|---|
| 0 | 0 | Transfer data from NVREG_ to VREG_ |
| 0 | 1 | Write to VREG_ |
| 1 | 0 | Write to NVREG_ |
| 1 | 1 | Write to NVREG and VREG_ |

### Table 3. DAC Write Selection

| R3 | R2 | R1 | R0 | FUNCTION |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | DAC0 |
| 0 | 0 | 0 | 1 | DAC1 |
| 1 | 1 | 1 | 1 | All DACs* |

**This option is only valid for a write to all volatile registers.*

### Table 4. Write-Command Summary

| COMMAND | START | ADDRESS BYTE | | ACK | COMMAND BYTE | | | | | | | | ACK | DATA BYTE | | | | | | | | ACK | STOP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | MSB | | | | | | | LSB | | |
| | | | R/$\overline{W}$ | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| Write VREG_ | S | | 0 | | 0 | 0 | 0 | 1 | R3 | R2 | R1 | R0 | | D7–D0 | | | | | | | | | P |
| Write All VREG_* | S | | 0 | | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | | D7–D0 | | | | | | | | | P |
| Write NVREG_ | S | | 0 | | 0 | 0 | 1 | 0 | R3 | R2 | R1 | R0 | | D7–D0 | | | | | | | | | P |
| Write VREG_ and NVREG_ | S | | 0 | | 0 | 0 | 1 | 1 | R3 | R2 | R1 | R0 | | D7–D0 | | | | | | | | | P |
| Transfer NVREG_ to VREG_ | S | | 0 | | 0 | 0 | 0 | 0 | R3 | R2 | R1 | R0 | | — | | | | | | | | | P |

**This option is only valid for a write to all volatile registers.*

### *Mute/Power-Down Mode*

The MAX5109 features software-controlled mute and power-down modes for each DAC. The power-down mode places the DAC output in a high-impedance state and reduces quiescent-current consumption (25µA (max) with all DACs powered-down).

Mute drives the selected DAC output to the corresponding REFL_ voltage. The volatile DAC registers retain data and the output returns to its previous state when mute is disabled. The MAX5109 also features an asynchronous $\overline{MUTE}$ input that mutes all DACs simultaneously.

The volatile and nonvolatile registers remain active while the MAX5109 is in mute and/or power-down modes. Writing to or reading from the volatile or nonvolatile registers does not remove the MAX5109 from mute or power-down mode. Writing or transferring data to the volatile registers while the device is muted or powered down updates the DAC outputs to the new state upon exiting mute or power-down mode.

# Nonvolatile, Dual, 8-Bit DACs with 2-Wire Serial Interface

### Table 5. Volatile and Nonvolatile Read Selection

| NONVOLATILE (NV) | VOLATILE (V) | FUNCTION |
|---|---|---|
| 0 | 1 | Read from VREG_ |
| 1 | 0 | Read from NVREG_ |

### Table 6. DAC Read Selection

| R3 | R2 | R1 | R0 | FUNCTION |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | DAC0 |
| 0 | 0 | 0 | 1 | DAC1 |

### Table 7. Mute/Power-Down Operation

| COMMAND | START | ADDRESS BYTE | | ACK | COMMAND BYTE | | | | | | | | ACK | DATA BYTE (MSB … LSB) | | | | | | | | ACK | STOP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | R/W | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| Write VCTL | S | | 0 | | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | | Control register* | | | | | | | | | P |
| Write NVCTL | S | | 0 | | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | | Control register* | | | | | | | | | P |
| Write VCTL and NVCTL | S | | 0 | | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | | Control register* | | | | | | | | | P |
| Transfer NVCTL to VCTL | S | | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | | Control register* | | | | | | | | | P |

**See Mute/Power-Down Control Register (Table 8).*

### Table 8. Mute/Power-Down Control Register

| | BIT IN REGISTER | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 (MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 (LSB) |
| CONTROLLING FUNCTION | X | X | Mute DAC1 | Mute DAC0 | X | X | Power-down DAC1 | Power-down DAC0 |

*X = Don't care.*

#### *Mute/Power-Down Register and Operation*

Separate nonvolatile and volatile control registers store and update the state of the mute/power-down mode for each DAC. Tables 7 and 8 show how to access and control each register. Register access is gained by setting control bits C3–C0 to 0100. Bits C5 and C4 indicate whether the nonvolatile or volatile control register is accessed. The volatile register maintains data while the device remains powered. The nonvolatile register maintains data even after power is removed. The MAX5109 starts up (power first applied) by transferring the mute/power-down modes from the nonvolatile control register to the volatile control register. The nonvolatile control register is set to 00 hex at the factory.

#### *Power-On Reset*

Power-on reset (POR) circuitry controls the initialization of the MAX5109. A POR loads the volatile registers with the data stored in the nonvolatile registers.

This initialization period takes 500µs (typ). During this time, the DAC outputs are held in mute mode. At the completion of the initialization period, the DAC outputs update in accordance with the data stored in the nonvolatile registers.

### DAC Data

The 8-bit DAC data is decoded as offset binary, MSB first, with 1 LSB = ($V_{REFH\_}$ - $V_{REFL\_}$) / 256, and converted into the corresponding analog voltage as shown in Table 9.

## Applications Information

### DAC Linearity and Offset Voltage

The output buffer can have a negative input offset voltage that would normally drive the output negative, but with no negative supply, the output remains at GND (Figure 9). Determine linearity using the end-point method, measuring between code 10 (0A hex) and code 240 (F0 hex) after calibrating the offset and gain error (Figure 9).

### External Voltage Reference

The MAX5109 features two reference inputs for each DAC (REFH_ and REFL_). REFH_ sets the full-scale voltage, while REFL_ sets the zero code output. A 460kΩ typical input impedance is independent of the code.

### Power Sequencing

The voltage applied to REFH_ and REFL_ should not exceed $V_{DD}$ at any time. If proper power sequencing is not possible, connect an external Schottky diode between REFH_, REFL_, and $V_{DD}$ to ensure compliance with the absolute maximum ratings. Do not apply signals to the digital inputs before the device is fully powered.

### Power-Supply Bypassing and Ground Management

Digital or AC transient signals on GND can create noise at the analog output. Return GND to the highest-quality ground available. Bypass $V_{DD}$, REFH_, and REFL_ to GND with a 0.1µF capacitor, located as close to the device as possible. Careful PC board ground layout minimizes crosstalk between the DAC outputs and digital inputs.

**Table 9. Unipolar Code Output Voltage**

| DAC CODE | OUTPUT VOLTAGE (V) |
|---|---|
| 1111 1111 | $\frac{255 \times (V_{REFH\_} - V_{REFL\_})}{256} + V_{REFL\_}$ |
| 1000 0000 | $\frac{128 \times (V_{REFH\_} - V_{REFL\_}}{256} + V_{REFL\_}$ |
| 0000 0001 | $\frac{(V_{REFH\_} - V_{REFL\_})}{256} + V_{REFL\_}$ |
| 0000 0000 | $V_{REFL\_}$ |

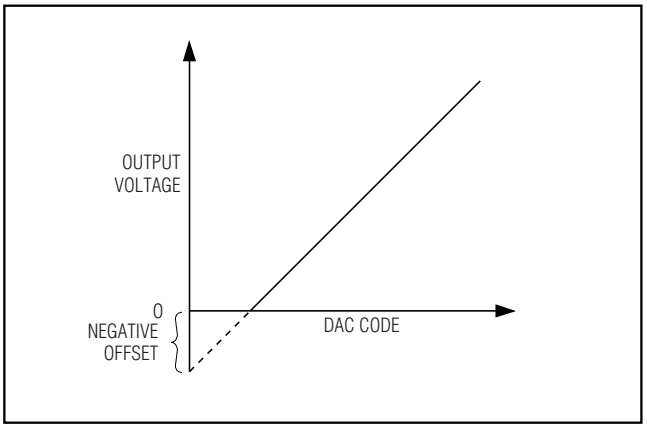
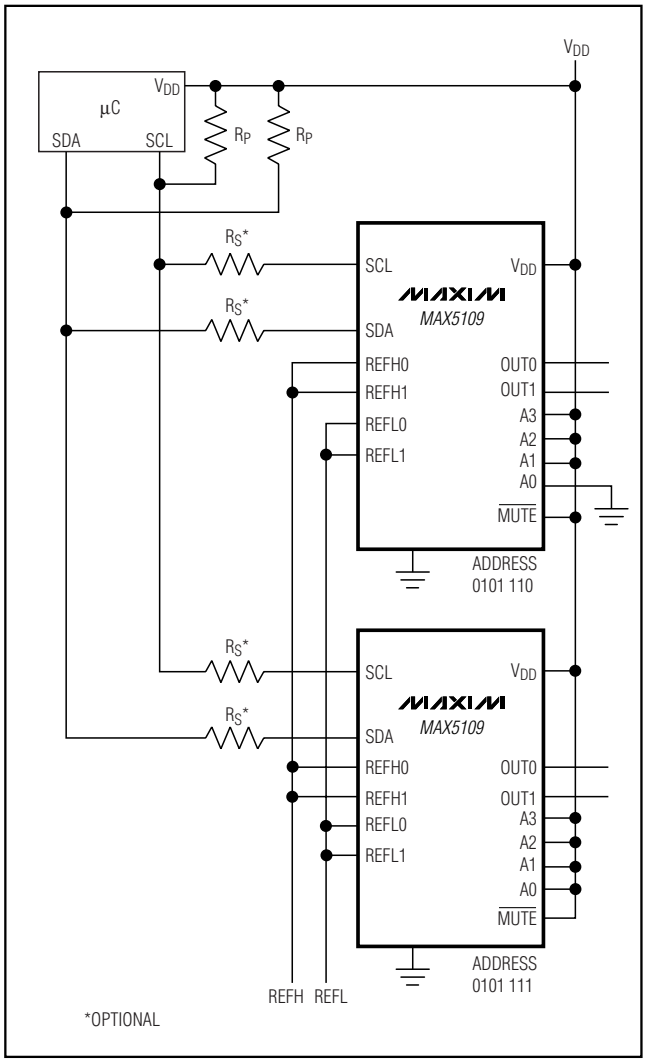


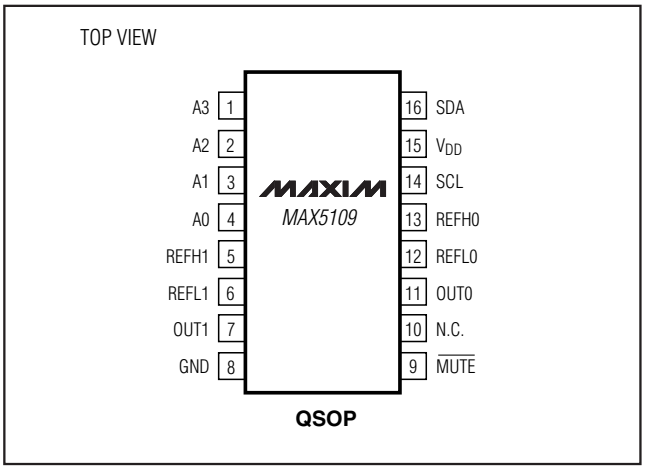

*Figure 9. Effect of Negative Offset (Single Supply)*

# Nonvolatile, Dual, 8-Bit DACs with 2-Wire Serial Interface

## Typical Operating Circuit




## Pin Configuration




## Chip Information

TRANSISTOR COUNT: 40,209

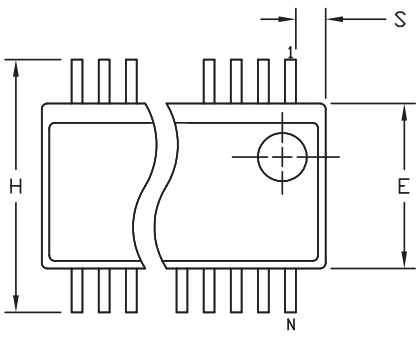
PROCESS: BiCMOS

# Nonvolatile, Dual, 8-Bit DACs with 2-Wire Serial Interface

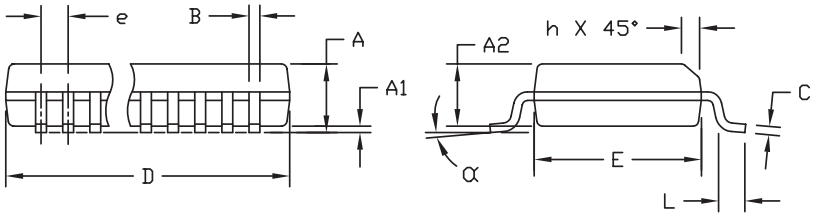
## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS




| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | .061 | .068 | 1.55 | 1.73 |
| A1 | .004 | .0098 | 0.102 | 0.249 |
| A2 | .055 | .061 | 1.40 | 1.55 |
| B | .008 | .012 | 0.20 | 0.30 |
| C | .0075 | .0098 | 0.191 | 0.249 |
| D | SEE VARIATIONS | | | |
| E | .150 | .157 | 3.81 | 3.99 |
| e | .025 BSC | | 0.635 BSC | |
| H | .230 | .244 | 5.84 | 6.20 |
| h | .010 | .016 | 0.25 | 0.41 |
| L | .016 | .035 | 0.41 | 0.89 |
| N | SEE VARIATIONS | | | |
| α | 0° | 8° | 0° | 8° |




VARIATIONS:

| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | N | |
| D | .189 | .196 | 4.80 | 4.98 | 16 | AB |
| S | .0020 | .0070 | 0.05 | 0.18 | | |
| D | .337 | .344 | 8.56 | 8.74 | 20 | AD |
| S | .0500 | .0550 | 1.270 | 1.397 | | |
| D | .337 | .344 | 8.56 | 8.74 | 24 | AE |
| S | .0250 | .0300 | 0.635 | 0.762 | | |
| D | .386 | .393 | 9.80 | 9.98 | 28 | AF |
| S | .0250 | .0300 | 0.635 | 0.762 | | |

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0055 | E | 1/1 |